

10/552948

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
1020 Dept. of PTO 13 OCT 2005

Applicant/Inventor: Chen et al.

Title: Read And Erase Verify Methods And Circuits Suitable For Low  
Voltage Non-Volatile Memories

Application No.: Unassigned

Filing Date: Herewith

Examiner: Unassigned

Group Art Unit: Unassigned

Docket No.: SNDK.284US1

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San Francisco, California  
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Mail Stop PCT  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**PRELIMINARY AMENDMENT FOR FILING UNDER 35 U.S.C. §371**

Sir:

Please preliminarily amend the above-identified patent application as set forth herein.